CLAIMS

1. A burst mode counter for use with a 2-bit prefetch memory device having an odd memory array designated by an odd column address and an even memory array designated by an even column address, the burst mode counter comprising:

a pre-settable column address counter changing count responsive to a clock signal, the counter having a starting count input receiving all but the least significant bit of a starting column address from which the counter increments or decrements, the counter further including a counter control input terminal receiving a counter control signal having a first value causing the counter to increment responsive to the clock signal or a second value causing the counter to decrement responsive to the clock signal; and

a counter control circuit receiving a mode signal having a first value indicative of a serial mode of operation and a second value indicative of an interleave mode of operation, the counter control circuit further receiving the least significant bit ("LSB") and the next to least significant bit ("NLSB") of the starting column address, the counter control circuit being operable to decode a value of "1" for the LSB and the first value of the mode signal and to generate the second value of the counter control signal responsive thereto, to decode a value of "1" for the NLSB and the second value of the mode signal and to generate the second value of the counter control signal responsive thereto, and to generate the first value of the counter control signal responsive to decoding other values of the LSB, NLSB and the mode signal.

2. The burst mode counter of claim 1 wherein the counter control circuit comprises a logic circuit.

3. The burst mode counter of claim 2 wherein the logic circuit comprises:

a first logic gate receiving the LSB of the starting column address and a signal indicative of the state of the mode signal;

a second logic gate receiving the NLSB of the starting column address and a signal indicative of the state of the mode signal; and

a third logic gate receiving respective outputs from the first and second logic gates.

4. A burst mode counter for use with a 2-bit prefetch memory device having an odd memory array designated by an odd column address and an even memory array designated by an even column address, the memory device being operable in an interleave mode, the burst mode counter comprising:

a pre-settable column address counter changing count responsive to a clock signal, the counter having a starting count input receiving all but the least significant bit of a starting column address from which the counter increments or decrements, the counter further including a counter control input terminal receiving a counter control signal having a first value causing the counter to increment responsive to the clock signal or a second value causing the counter to decrement responsive to the clock signal; and

a counter control circuit receiving the next to least significant bit ("NLSB") of the starting column address, the counter control circuit being operable to generate the second value of the counter control signal responsive to a value of "1" for the NLSB, and to generate the first value of the counter control signal responsive to a value of "0" for the NLSB.

5. The burst mode counter of claim 4 wherein the counter control circuit comprises a logic circuit.

6. A burst mode counter for use with a 2-bit prefetch memory device having an odd memory array designated by an odd column address and an even memory array designated by an even column address, , the memory device being operable in a serial mode, the burst mode counter comprising:

a pre-settable column address counter changing count responsive to a clock signal, the counter having a starting count input receiving all but the least significant bit of a starting column address from which the counter increments or decrements, the counter further including a counter control input terminal receiving a counter control signal having a first

value causing the counter to increment responsive to the clock signal or a second value causing the counter to decrement responsive to the clock signal; and

a counter control circuit receiving the least significant bit ("LSB") of the starting column address, the counter control circuit being operable to generate the second value of the counter control signal responsive to a value of "1" for the LSB, and to generate the first value of the counter control signal responsive to a value of "0" for the LSB.

7. The burst mode counter of claim 6 wherein the counter control circuit comprises a logic circuit.

8. A dynamic random access memory ("DRAM"), comprising:

an even array of memory cells arranged in rows and columns;

an odd array of memory cells arranged in rows and columns;

a row decoder coupled to receive a row address and being operable to activate a row of memory cells corresponding to the row address;

a column address decoder coupled to receive a column address and to select a column of memory cells in each array corresponding to the column address;

a data path coupled between the memory arrays and a data bus;

a command decoder operable to receive memory commands from a command bus and to generate control signals corresponding to respective memory commands;

a pre-settable burst counter changing count responsive to a clock signal, the burst counter having a count input receiving all but the least significant bit of a column address from which the counter increments or decrements, the burst counter further including a counter control input terminal receiving a counter control signal having a first value causing the burst counter to increment responsive to the clock signal or a second value causing the burst counter to decrement responsive to the clock signal; and

a counter control circuit receiving a mode signal having a first value indicative of a serial mode of operation and a second value indicative of an interleave mode of operation, the counter control circuit further receiving the least significant bit ("LSB") and the next to least significant bit ("NLSB") of the column address, the counter control circuit being

operable to decode a value of "1" for the LSB and the first value of the mode signal and to generate the second value of the counter control signal responsive thereto, to decode a value of "1" for the NLSB and the second value of the mode signal and to generate the second value of the counter control signal responsive thereto, and to generate the first value of the counter control signal responsive to decoding other values of the LSB, NLSB and the mode signal.

9. The DRAM of claim 8, wherein the DRAM comprises a synchronous DRAM.

10. The DRAM of claim 8 wherein the counter control circuit comprises a logic circuit.

11. The DRAM of claim 10 wherein the logic circuit comprises:

a first logic gate receiving the LSB of the column address and a signal indicative of the state of the mode signal;

a second logic gate receiving the NLSB of the column address and a signal indicative of the state of the mode signal; and

a third logic gate receiving respective outputs from the first and second logic gates.

12. A dynamic random access memory ("DRAM") operable in an interleave mode, the DRAM comprising:

an even array of memory cells arranged in rows and columns;

an odd array of memory cells arranged in rows and columns;

a row decoder coupled to receive a row address and being operable to activate a row of memory cells corresponding to the row address;

a column address decoder coupled to receive a column address and to select a column of memory cells in each array corresponding to the column address;

a data path coupled between the memory arrays and a data bus;

a command decoder operable to receive memory commands from a command bus and to generate control signals corresponding to respective memory commands;

a pre-settable burst counter changing count responsive to a clock signal, the burst counter having a count input receiving all but the least significant bit of a column address from which the burst counter increments or decrements, the burst counter further including a counter control input terminal receiving a counter control signal having a first value causing the burst counter to increment responsive to the clock signal or a second value causing the burst counter to decrement responsive to the clock signal; and

a counter control circuit receiving the next to least significant bit ("NLSB") of the column address, the counter control circuit being operable to generate the second value of the counter control signal responsive to a value of "1" for the NLSB, and to generate the first value of the counter control signal responsive to decoding a value of "0" for the NLSB.

13. The DRAM of claim 12, wherein the DRAM comprises a synchronous DRAM.

14. The DRAM of claim 12 wherein the counter control circuit comprises a logic circuit.

15. A dynamic random access memory("DRAM") operable in a serial mode, the DRAM, comprising:

an even array of memory cells arranged in rows and columns;

an odd array of memory cells arranged in rows and columns;

a row decoder coupled to receive a row address and being operable to activate a row of memory cells corresponding to the row address;

a column address decoder coupled to receive a column address and to select a column of memory cells in each array corresponding to the column address;

a data path coupled between the memory arrays and a data bus;

a command decoder operable to receive memory commands from a command bus and to generate control signals corresponding to respective memory commands; and

a pre-settable burst counter changing count responsive to a clock signal, the burst counter having a count input receiving all but the least significant bit of a column address from which the counter increments or decrements, the burst counter further including a counter control input terminal receiving a counter control signal having a first value causing the burst counter to increment responsive to the clock signal or a second value causing the burst counter to decrement responsive to the clock signal; and

a counter control circuit receiving receiving the least significant bit ("LSB") of the column address, the counter control circuit being operable to generate the second value of the counter control signal responsive to a value of "1" for the LSB, and to generate the first value of the counter control signal responsive to a value of "0" for the LSB.

16. The DRAM of claim 15, wherein the DRAM comprises a synchronous DRAM.

17. The DRAM of claim 15 wherein the counter control circuit comprises a logic circuit.

18. A computer system, comprising:

computer circuitry operable to perform computing functions;

at least one input device coupled to the computer circuitry;

at least one output device coupled to the computer circuitry;

at least one data storage devices coupled to the computer circuitry; and

a dynamic random access memory, comprising

an even array of memory cells arranged in rows and columns;

an odd array of memory cells arranged in rows and columns;

a row decoder coupled to receive a row address and being operable to activate a row of memory cells corresponding to the row address;

a column address decoder coupled to receive a column address and to select a column of memory cells in each array corresponding to the column address;

a data path coupled between the memory arrays and a data bus;

a command decoder operable to receive memory commands from a command bus and to generate control signals corresponding to respective memory commands;

a pre-settable burst counter changing count responsive to a clock signal, the burst counter having a count input receiving all but the least significant bit of a column address from which the counter increments or decrements, the burst counter further including a counter control input terminal receiving a counter control signal having a first value causing the burst counter to increment responsive to the clock signal or a second value causing the burst counter to decrement responsive to the clock signal; and

a counter control circuit receiving a mode signal having a first value indicative of a serial mode of operation and a second value indicative of an interleave mode of operation, the counter control circuit further receiving the least significant bit ("LSB") and the next to least significant bit ("NLSB") of the column address, the counter control circuit being operable to decode a value of "1" for the LSB and the first value of the mode signal and to generate the second value of the counter control signal responsive thereto, to decode a value of "1" for the NLSB and the second value of the mode signal and to generate the second value of the counter control signal responsive thereto, and to generate the first value of the counter control signal responsive to decoding other values of the LSB, NLSB and the mode signal.

19. The computer system of claim 18, wherein the DRAM comprises a synchronous DRAM.

20. The computer system of claim 18 wherein the counter control circuit comprises a logic circuit.

21. The computer system of claim 20 wherein the logic circuit comprises:

a first logic gate receiving the LSB of the column address and a signal indicative of the state of the mode signal;

a second logic gate receiving the NLSB of the column address and a signal indicative of the state of the mode signal; and

a third logic gate receiving respective outputs from the first and second logic gates.

22. A computer system, comprising:

computer circuitry operable to perform computing functions;

at least one input device coupled to the computer circuitry;

at least one output device coupled to the computer circuitry;

at least one data storage devices coupled to the computer circuitry; and

a dynamic random access memory operable in an interleave mode, the dynamic random access memory comprising

an even array of memory cells arranged in rows and columns;

an odd array of memory cells arranged in rows and columns;

a row decoder coupled to receive a row address and being operable to activate a row of memory cells corresponding to the row address;

a column address decoder coupled to receive a column address and to select a column of memory cells in each array corresponding to the column address;

a data path coupled between the memory arrays and a data bus;

a command decoder operable to receive memory commands from a command bus and to generate control signals corresponding to respective memory commands;

a pre-settable burst counter changing count responsive to a clock signal, the burst counter having a count input receiving all but the least significant bit of a column address from which the burst counter increments or decrements, the burst counter further including a counter control input terminal receiving a counter control signal having a first value causing the burst counter to increment responsive to the clock signal or a second value causing the burst counter to decrement responsive to the clock signal; and

a counter control circuit receiving the next to least significant bit ("NLSB") of the column address, the counter control circuit being operable to generate the second value of the counter control signal responsive to a value of "1" for the NLSB and to generate the first value of the counter control signal responsive to a value of "1" for the NLSB.

23. The computer system of claim 22, wherein the DRAM comprises a synchronous DRAM.

24. The computer system of claim 22 wherein the counter control circuit comprises a logic circuit.

25. A computer system, comprising:

computer circuitry operable to perform computing functions;

at least one input device coupled to the computer circuitry;

at least one output device coupled to the computer circuitry;

at least one data storage devices coupled to the computer circuitry; and

a dynamic random access memory operable in a serial mode, the dynamic random access memory comprising

an even array of memory cells arranged in rows and columns;

an odd array of memory cells arranged in rows and columns;

a row decoder coupled to receive a row address and being operable to activate a row of memory cells corresponding to the row address;

a column address decoder coupled to receive a column address and to select a column of memory cells in each array corresponding to the column address;

a data path coupled between the memory arrays and a data bus;

a command decoder operable to receive memory commands from a command bus and to generate control signals corresponding to respective memory commands; and

a pre-settable burst counter changing count responsive to a clock signal, the burst counter having a count input receiving all but the least significant bit of a column address from which the counter increments or decrements, the burst counter further including a counter control input terminal receiving a counter control signal having a first value causing the burst counter to increment responsive to the clock signal or a second value causing the burst counter to decrement responsive to the clock signal; and

a counter control circuit receiving the least significant bit ("LSB") of the column address, the counter control circuit being operable to generate the second value of the counter control signal responsive to a value of "1" for the LSB and to generate the first value of the counter control signal responsive to a value of "0" for the LSB.

26. The computer system of claim 25, wherein the DRAM comprises a synchronous DRAM.

27. The computer system of claim 25 wherein the counter control circuit comprises a logic circuit.

28. A method of burst-mode addressing a 2-bit prefetch memory device operable in either a serial mode or an interleave mode, comprising:

in the serial mode, incrementing a column address from a starting column address when a least significant bit ("LSB") of the starting column address is a logic "0";

in the serial mode, decrementing a column address from the starting column address when the LSB of the starting column address is a logic "1";

in the interleave mode, incrementing a column address from the starting column address when a next to least significant bit ("NLSB") of the starting column address is a logic "0"; and

in the interleave mode, decrementing a column address from the starting column address when the NLSB of the starting column address is a logic "1".

29. A method of burst-mode addressing a 2-bit prefetch memory device operable in an interleave mode, comprising:

incrementing a column address from the starting column address when a next to least significant bit ("NLSB") of the starting column address is a logic "0"; and

decrementing a column address from the starting column address when the NLSB of the starting column address is a logic "1".

30. A method of burst-mode addressing a 2-bit prefetch memory device operable in a serial mode, comprising:

incrementing a column address from a starting column address when a least significant bit ("LSB") of the starting column address is a logic "0"; and

decrementing a column address from the starting column address when the LSB of the starting column address is a logic "1".

32. A method of controlling a bust counter for a memory device operable in a 2-bit prefetch mode, the method comprising:

in a serial operating mode, controlling the count direction of the bust counter responsive to the state of the least significant bit ("LSB") of a starting column address; and

in an interleave operating mode, controlling the count direction of the bust counter responsive to the state of the next to least significant bit ("NLSB") of the starting column address.

33. The method of claim 32 wherein the act of controlling the count direction of the bust counter responsive to the LSB in the serial operating mode comprises:

incrementing a column address from the starting column address when the LSB is a logic "0"; and

decrementing a column address from the starting column address when the LSB is a logic "1".

34. The method of claim 32 wherein the act of controlling the count direction of the bust counter responsive to the NLSB in the interleave operating mode comprises:

incrementing a column address from the starting column address when the NLSB is a logic "0"; and

decrementing a column address from the starting column address when the NLSB is a logic "1".